REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-6, 9-19 and 28-31 are currently being prosecuted. The Examiner is respectfully requested to reconsider her rejections in view of the amendments and remarks as set forth below.

Rejection Under 35 USC §112

Claims 9-19 stand rejected under 35 USC §112, second paragraph as being indefinite. This rejection is respectfully traversed.

Claims 9 and 14-18 have now been amended to overcome the problems noted by the Examiner. In claim 9, the objectionable phrase has been removed and instead the IC and coil are now recited as being disposed at the center portion of a plane of the substrate. This language and the previous language was intended to state that the two parts are disposed at the center of the substrate, but in the lateral or planar direction as opposed to the thickness direction.

In regard to claim 14, the objectionable language has been changed to more clearly state that the substrate has three layers bonded together. Although, the Examiner has not objected to claim 16 and 17, the corresponding language has been changed in those claims as well.

In regard to claim 18, the language has been replaced with "a circle in said plane of said substrate". This language has also been changed in claim 15 which has a similar problem. It is believed that these changes overcome this rejection.

Rejection Under 35 USC §102

Claims 9, 11-13 and 30 stand rejected under 35 USC §102 as being anticipated over Droz (U.S. Patent 6,176,010). This rejection is respectfully traversed.

The Examiner states that Droz shows a substrate having an IC element mounted thereon where the IC element is formed integrally with the coil and where the two are disposed at a center portion of the substrate. The Examiner especially refers to Fig. 8 of the reference. Applicants submit that the Examiner has misread the reference and that in fact the reference does not show the features indicated by the Examiner.

In particular, the Examiner states that the IC element is formed integrally with the antenna coil. As seen in Figs. 8 and 9, the IC element 25 is placed in accommodation 24 which appears to be some sort of recess in the substrate. However, the inductive element 23 is formed on the outer part of the substrate. As indicated in column 6, lines 28-30, the accommodation is provided in a portion of the lower sheet not occupied by the conducting paths. The ends of the inductive element 23 are connected to the integrated circuit, but they are not integrally formed. Further, the Examiner states that the IC element and the coil are disposed at the center portion of the substrate. It is noted that IC element is not formed in the direct center, but is slightly offset to one side. Even ignoring this, it is clear that the coil is not formed at the center portion at all. Instead the coil is formed around the periphery of the substrate leaving the center portion open except for the IC element.

Claim 9 describes an information carrier having a combination of elements including a substrate with an IC element mounted thereon, where the element is integrally formed with an antenna coil as a composite and where the element and the coil are disposed at the

center portion of the plane of the substrate. In the IC element of the present invention, the coils are connected to the circuit and both are formed integrally on a semiconductor wafer as a composite.

The Droz reference does not show this combination of elements since it does not disclose an IC element integrally formed with the coil as a composite and since the element and coil are not disposed at the center portion of the substrate. Also, this reference is not the kind of structure where the antenna is formed on the chip, but where the antenna, which is large compared to the chip, is formed independently and afterwards connected to a terminal of the chip. For these reasons, Applicants submit that claim 9 defines over this reference.

The Examiner also rejected claims 11-13 and 30 over the same reference. These claims depend from claim 9 and as such are also considered to be allowable. Further, in regard to claim 30, Applicants submit that the Examiner is completely incorrect in stating that the entirety of the coil is formed on the surface of the IC element. While the coil is formed on the surface of the substrate, it is not formed on any portion on the surface of the IC element. Certainly, the entirety of the coil is not formed on the surface. For this reason, Applicants submit that claim 30 is further allowable.

Rejection Under 35 USC §103

Claims 1, 2, 4-6, 19, 28 and 29 stand rejected under 35 USC §103 as being obvious over Droz in view of Inoue (U.S. Patent 4,960,983). This rejection is respectfully traversed.

Claim 1 describes an IC element having a combination of elements including a coil which is integrally formed with the IC element and where the conductor of the coil has a plurality of adjacent conductive layers including either a metal-sputtered layer or a metal-evaporated layer and additionally a metal-plated layer. Applicants submit that this combination of elements is not obvious over the two references cited by the Examiner.

The Examiner states that Droz shows a conductor implemented in a multi-layer structure. While the Examiner is correct that the embodiment of Fig. 6 shows a plurality of conducting layers 2, 2', 2", 2"', these are insulated by adhesive layers 4, 4', 4", 4"'. As indicated at column 4, lines 45-48, these adhesive layers act as insulators between the metallic layers. Also, as indicated in column 3, lines 44-46, the layer of adhesive must be perfectly insulating electrically. Thus, in this system the individual layers form separate electrical devices rather than being combined into a single conductor. This difference is now emphasized in claim 1 where the conductor is described as having a plurality of adjacent conductive layers. In the Droz reference, while there are a plurality of conductive layers, they are not adjacent, but rather separated by insulating layers. Also, in the reference, this is not a single conductor, but rather multiple separate conductors.

Also, claim 1, like claim 9 as described above, describes that the IC element and the coil are integrally formed as a composite. As described above, in the Droz reference, the IC element is separate from the coil and not integrally formed therewith.

The Examiner cited the Inoue reference to show the use of sputtering. However, even if this reference does show this feature, the combination of the two references still fails to show the combination of elements described in claim 1. Further, Inoue shows an IC

chip in which the coil is formed on the IC element for communicating with an external apparatus in a non-contact manner. However, Inoue does not disclose a multi-layer structure nor an arrangement where the chip and coil are formed integrally as a composite on a semiconductor wafer. Accordingly, Applicants submit that claim 1 is patentable over this combination of references.

The Examiner also rejected claims 2, 4-6, 28 and 29 over this combination of references. These claims depend from claim 1 and are allowable for the same reasons as cited above. In addition, claim 4 states that the corner portions are chamfered. This feature is not seen in the Droz reference as suggested by the Examiner. While the coil is in a rectangular spiral pattern, Applicants do not see any corner portions which have been chamfered. In regard to claim 28, Applicants submit that neither of the references teach this feature. The Examiner has suggested that this would be obvious in view of the description in Inoue for sputtering metal layers. However, Applicants submit that there is no motivation to have the specific relationship between the two resistances as specified in claim 28.

In regard to claim 29, the Examiner states in the last two lines of page 9 of the Action that Droz fails to show that the entirety of the coil is formed on the surface of the IC element. However, the Examiner does not state why this feature would be obvious and does not describe how this is found in Inoue or in any other reference. Applicants submit that the reference does not teach the coil being formed on the surface of the IC element as described and accordingly this claim is clearly allowable.

The Examiner also rejected claim 19 over this combination of elements. This claims depends from claim 9 so that Applicants submit that claim 19 is allowable based on its dependency.

Claim 3 stands rejected under 35 USC §103 as being obvious over Droz in view of Inoue and McDonough et al (U.S. Publication 2001/0044013).

Claim 10 stands rejected under 35 USC §103 as being obvious over Droz et al in view of Masahiko (U.S. Patent 5,852,289).

Claims 14 and 15 stand rejected under 35 USC §103 as being obvious over Droz et al in view of McDonough et al.

Claims 16-18 stand rejected under 35 USC §103 as being obvious over Droz et al in view of Fidalgo (U.S. Patent 5,598,032).

These rejections are all respectfully traversed. Applicants submit that even if the additional references teach the features indicated, these claims are allowable based on their dependency from allowable claims 1 and 9. In addition, these claims also recite other features which taken in conjunction with the combination of elements in the independent claims are further allowable.

Thus, claim 3 requires that the coil is formed on the surface of the IC element and having input/output terminals. Applicants submit that none of the references teach the concept of the coil being formed on the surface of the element and the combination of this feature with the input/output terminals. Accordingly, claim 3 is additionally allowable.

Claims 10 and 14-18 describe additional features of the substrate and the mounting of the element therein.

It is further noted that in paragraph 14 the Examiner has repeated the rejection of claim 19 which was also included in the rejection of paragraph 9 as found on page 8. Accordingly, the comments in regard to this claim above are repeated.

Applicants have added claim 31 which describes the multi-layer arrangement of the conductor in the coil in a fashion similar to that described in claim 1, but as a dependent claim which depends from claim 9. This claim is also considered to be allowable for the reasons recited above regarding this feature in claim 1 and also based on its dependency from claim 9.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner either alone or in combination. In view of the above amendment and remarks, reconsideration of the rejections and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicants respectfully petition for a three (3) month extension of time for filing a response in connection with the present application and the required fee of $930 is being filed concurrently herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment(s): Corrected Formal Drawings